PATENT
Docket No.: SK00002C1(00CXT0656C1)
10/691,115

AMENDMENTS

TO THE CLAIMS

1. (original): A constant current bias circuit comprising:

an at least one resistor; and

a bias voltage input terminal for receipt of a bias voltage connected to the at least one resistor by an electrical path resulting in a bias current when the bias voltage is present.

2. (original): The constant current bias circuit of claim 1, further comprising:

a clamp circuit coupled by an electrical path to the at least one resistor that provides a minimum current.

3. (original): The constant current bias circuit of claim 1, wherein the bias current is in a linear relationship with the bias voltage.

4. (original): The constant current bias circuit of claim 1, further comprising:

a circuit having a plurality of components electrically coupled to the at least one resistor in receipt of the bias current.

5. (currently amended): The constant current bias circuit of claim 4, wherein the at least one resistor is in a first material in a substrate and at least one component of

the plurality of components is a second material ~~is~~ in the substrate and different from the first material.

6. (original): The constant current bias circuit of claim 5, wherein the first material is Complementary Metal Oxide Semiconductor fabrication material.

7. (original): The constant current bias circuit of claim 6, wherein the second material is Gallium Arsenide Semiconductor fabrication material.

8. (original): The constant current bias circuit of claim 4, wherein the circuit is a single stage amplifier.

9. (original): The constant current bias circuit of claim 4, wherein the circuit is a multi-stage amplifier.

10. (original): The constant current bias circuit of claim 1, further comprising a feedback loop that maintains a quiescent bias for a transistor equal to a reference current, wherein the reference current is mirrored from the bias current.

11. (original): A constant current bias circuit comprising:

an at least one resistor; and

means for receiving a bias voltage connected to the at least one resistor by an electrical path resulting in a bias current when the bias voltage is present.

12. (original): The constant current bias circuit of claim 11, further comprising:

means for providing a minimum bias current coupled by an electrical path to the at least one resistor.

13. (original): The constant current bias circuit of claim 11, wherein the bias current is in a linear relationship with the bias voltage.

14. (original): The constant current bias circuit of claim 11, further comprising:

a circuit having a plurality of components electrically coupled to the at least one resistor in receipt of the bias current.

15. (currently amended): The constant current bias circuit of claim 14, wherein the at least one resistor is in a first material in a substrate and at least one component of the plurality of components is a second material ~~is~~ in the substrate and different from the first material.

16. (original): The constant current bias circuit of claim 15, wherein the first material is Complementary Metal Oxide Semiconductor fabrication material.

17. (original): The constant current bias circuit of claim 16, wherein the second material is Gallium Arsenide Semiconductor fabrication material.

18. (original): The constant current bias circuit of claim 14, wherein the circuit is a single stage amplifier.

19. (original): The constant current bias circuit of claim 14, wherein the circuit is a multi-stage amplifier.

20. (original): The constant current bias circuit of claim 11, further comprising a means for generating a feedback loop to maintain a quiescent bias for a transistor equal to a reference current, wherein the reference current is mirrored from the bias current.

21. (original): A method for current bias circuit, comprising:

receiving an input bias voltage; and

generating a bias current by at least one resistor being in receipt of the input bias voltage.

22. (original): The method of claim 21, further comprising:

determining if the bias current is above a predetermined threshold.

23. (original): The method of claim 22, further comprising:

activating a clamp circuit to assure the bias current is above a predetermined threshold.

24. (currently amended): The method of claim 21, further comprising:

mirroring the bias current I_{ref} to a base current I_{base} by a predetermined ~~ration~~ratio.

25. (currently amended): The method of claim 21, further comprising:

receiving the bias current at a transistor in a first material different from a second material, wherein the bias current was generated in ~~a~~the second material.

26. (currently amended): The method of claim 25, wherein the second material is CMOS and shares a substrate with the ~~second~~first material.

27. (original): The method of claim 21, further comprising:

maintaining a feedback loop of a quiescent bias for a transistor equal to the reference current, wherein the reference current is mirrored from the bias current.